

1. For the 4X4 bit barrel shifter, the regularity factor is given by
 - a. 8
 - b. 4
 - c. 2
 - d. 16
2. The level of any particular design can be measured by
 - a. SNR
 - b. Ratio of amplitudes
 - c. regularity
 - d. quality
3. In tackling the design of system the more significant property is
 - a. logical operations
 - b. test ability
 - c. topological properties
 - d. nature of architecture
4. Any bit shifted out at one end of data word will be shifted in at the other end of the word is called
 - a. end-around
 - b. end-off
 - c. end-less
 - d. end-on
5. In the VLSI design the data and control signals of a shift register flow in
 - a. horizontally and vertically
 - b. vertically and horizontally
 - c. both horizontally
 - d. both vertically
6. The subsystem design is classified as
 - a. first level
 - b. top level
 - c. bottom level
 - d. leaf-cell level
7. The larger system design must be partitioned into a subsystems design such that
 - a. minimum interdependence and inter connection
 - b. complexity of interconnection

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c. maximum interdependence

d. arbitrarily chosen

8. To simplify the subsystem design, we generally used the

a. interdependence

b. complex interconnections

c. regular structures

d. standard cells

9. System design is generally in the manner of

a. down-top

b. top-down

c. bottom level only

d. top level only

10. Structured design begins with the concept of

a. hierarchy

b. down-top design

c. bottom level design

d. complex function design

11. Any general purpose n-bit shifter should be able to shift incoming data by up to number of places are

a. n

b. $2n$

c. $n-1$

d. $2n-1$

12. For a four bit word, a one-bit shift right is equivalent to a

a. two bit shift left

b. three-bit shift left

c. one bit shift left

d. four-bit shift left

13. The type of switch used in shifters is

a. line switch

b. transistor type switch

c. crossbar switch

d. gate switch

14. The representation of basic cell used in multiplier is

= latch

GFA = gated full adder

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P_i = partial product sum in

P = partial product sum out

C_i = carry in

C = carry out

d = line required for two's complement operation

a. Shown in figure (a)

Figure(a)

b. Shown in figure (a)

Figure(a)

c. Shown in figure (a)

Figure(a)

d. Shown in figure (a)

Figure(a)

15.

a.

b.

c.

d. shown in figure (a)

Figure(a)

16. The carry chain in adder is consist with

a. cross-bar swith

b. transmission gate

c. bus interconncection

d. pass transistors

17. VLSI design of adder element basically requires

a. EX-OR gate, Not and OR gates

b. multiplexers, inverter circuit and communication paths

c. multiplexers, EX-OR and NAND gates

d. inverter circuits and communication paths

18. The number of basic cells required for an n -bit X n -bit multiplier is

a. $(3n+1)$

b. $(3n+1)2n$

c.

d.

19. The heart of the ALU is

a. Register

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b. adder

c. control bus

d. I/O port

20. In the VLSI design the adder requirements may be stated as

a. if $A_k = B_k$ then else

b. if then else

c. if $A_k = B_k$ then else

d. if $A_k = B_k$ then else $S =$

21. In the VLSI design the carry of adder requirements may be stated as

a. if then $C =$ & then $C =$

b. if then $C =$ & then $C =$

c. if then $C =$ & then $C =$

d. if then $C =$ & then $C =$

22. Carry line in adder must be buffered after or before each adder element because

a. slow response of series pass transistors

b. slow response of parallel line

c. fast response of parallel pass transistors

d. fast response of series line

23. The ALU logical functions can be obtained by a suitable switching of the

a. carry line between adder elements

b. sum line between adder elements

c. carry line between shifter & buffer

d. sum line between shifter & buffer

24. To fast an arithmetic operations, the multipliers and dividers is to use architecture of

a. parallel

b. serial

c. pipelined

d. switched

25. The logical expressions for the two output signals in terms of the four input signals in comparator for VLSI design are

A_i & B_i are two numbers to be compared

C_{i+1} & D_{i+1} are inputs from o/p of previous stage

C_i & D_i are the outputs of the current stage

a.

b.

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c.

d.

26. The representation of function of parity generator is

a.

b.

c.

d.

27. The number of bits increases in comparator then the

a. height increases

b. width grows linearly

c. width reduces linearly

d. height reduces

28. The representation of a basic one bit cell is

a. Shown in figure (a)

Figure(a)

b. Shown in figure (a)

Figure(a)

c. Shown in figure (a)

Figure(a)

d. Shown in figure (a)

Figure(a)

29. The standard cell for an n-bit parity generator is

a. n-1 bit cell

b. one bit cell

c. two bit cell

d. n+1 bit cell

30. The parity information is passed from one cell to the next and is modified or not by a cell depending on the state of the

a. previous information

b. output line

c. input lines

d. next information

31. The parity information (p_i) passed from one cell to the next is modified when the input line (A_i) is at the state of

a. zero

b. $\overline{A_i}$

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c. one

d. independent of input line state

32. When cells of parity generator are butted together (indicate false statement)

a. design rule errors are not present

b. wastage of area is avoided

c. inlet and outlet points of cells must be match up

d. layer and position match is not necessary

33. The standard cell representation of comparator in VLSI design is

A_i and B_i are two numbers to be compared.

C_{i+1} and D_{i+1} are inputs from outputs of previous stage

C_i and D_i are the outputs of the currents stage.

a. Shown in figure (a)

Figure(a)

b. Shown in figure (a)

Figure(a)

c. Shown in figure (a)

Figure(a)

d. Shown in figure (a)

Figure(a)

34. The two output signals of comparator remain at zero as long as the two bits being compared are

a. same

b. zero

c. one

d. different

35. In the comparator the two inputs if $A > B$ then the outputs are

a. $C_i = 0$ & $D_i = 1$

b. $C_i = 1$ & $D_i = 0$

c. $C_i = 1$ & $D_i = 1$

d. $C_i = 0$ & $D_i = 0$

36. In the comparator the two inputs if $A < B$ then the outputs are

a. $C_i = 0$ & $D_i = 0$

b. $C_i = 1$ & $D_i = 1$

c. $C_i = 0$ & $D_i = 1$

d. $C_i = 1$ & $D_i = 0$

37. The width of n bit comparator is

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Where w is the width of leaf cell

- a. $n w$
- b. w
- c. $(n-1) w$
- d. n

38. The main draw back of asynchronous counter with respect to VLSI is

- a. The output change with respect to clock edge
- b. counter stages are cascaded
- c. the last counter stage to settle can be quite large
- d. clocking of each stage is carried out by the previous stage

39. ONE/ZERO detection circuits for word width of less than 32 bits is the

- a. pseudo-nMOS OR gate
- b. pseudo-nMOS NOT gate
- c. pseudo-nMOS NOR gate
- d. nmos OR gate

40. The delay from the last changing output to the ripple zero/one detector is a

- a. constant one gate delay
- b. variable delay
- c. greater than two gate delays
- d. constantly increasing delay

41. The speed that synchronous up/down counter can operate is determined by the

- a. ripple-carry time from the LSB to MSB
- b. substantially the clock time
- c. delay of registers
- d. settling time of counter

42. Detecting all ones or all zeros on wide words require

- a. large fanout AND or OR gates
- b. large fanin AND or OR gates
- c. large fan in EX-NOR or EX-OR gates
- d. large fanout NOR or NAND gates

43. In zero/one detector, the delay to the output is proportional to
(N is bit width of the word)

- a. N
- b. N^2
- c. $-\log N$
- d. $\log N$

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44. Self-loading of large word widths in ONE/ZERO detectors is avoided by
- a. split into 8 or 16 bit chunks
 - b. use large fan in gates
 - c. use large word width pseudo-nMOS NOR gates
 - d. use large fanout gates
45. Binary counters are used to cycle through a sequence of
- a. Decimal numbers
 - b. binary numbers
 - c. hexa decimal numbers
 - d. octal numbers
46. An asynchronous counter has outputs that change at
- a. varying times with respect to the clock edge
 - b. substantially the same clock time
 - c. twice that of the clock edge time
 - d. half time of the clock
47. The clocking of each stage of ripple counter is carried out by the
- a. common clock
 - b. previous counter stage
 - c. connected positive and negative cycles alternately
 - d. master-slave flip-flop
48. Proper placement of memory elements makes maximum use of the
- a. available clock period
 - b. cost of area
 - c. power dissipation
 - d. parasitics
49. A design that requires high density memory is usually
- a. a single chip
 - b. on chip
 - c. partitioned into several chips
 - d. DRAMS
50. Random access memory at the chip level is classed as memory that has
- a. an access time dependent of the physical location of the data
 - b. an access time independent of the physical location of the data
 - c. reading or writing of a particular datum with address
 - d. examines a data word and compares this data with internally stored data
51. The following memory examines data word and compares this data with

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internally stored data

- a. serial access memory
- b. random access memory
- c. content addressable memory
- d. shift registers memory

52. The main characteristics of on chip memory is

- a. small and slow
- b. large and slow
- c. small and faster
- d. large and faster

53. DRAM has a

- a. smaller layout and uses large power
- b. smaller layout and uses less power
- c. more power and slower
- d. more power and faster

54. SRAM has a

- a. faster, more power and larger
- b. slower, more power and larger
- c. faster, less power and smaller
- d. faster less power and larger

55. On chip memory is comes under the category of

- a. high density memory
- b. medium density memory
- c. low density memory
- d. large density memory

56. On chip memory usually in the order of

- a. 10k bytes
- b. 50k bytes
- c. 1k bytes
- d. 100 k bytes

57. The simplest and safest way to use memory in a system is to treat it as a

- a. sequential component
- b. combinational component
- c. decoders
- d. NOR gates

58. Serial access memory at the chip level is classed as memory that has

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- a. shift registers
 - b. counters
 - c. accesstime is independent of location of data
 - d. internally stored data is used
59. The PLA provides a systematic and regular way of implementing multiple output functions of n variables in
- a. POS form
 - b. SOP form
 - c. complex form
 - d. simple form
60. V (input variables) $\times$ P (product terms) PLA is to maintain generality within the constraints of its dimensions then for
- a. AND gate have n inputs and output OR gate must have P inputs
 - b. AND gate have P inputs and output OR gate must have n inputs
 - c. Both AND gate and OR gate have n inputs
 - d. both AND and or gates have P inputs
61. A MOS PLA is realized by using the gate of
- a. AND
 - b. OR
 - c. AND-OR
 - d. NOR
62. A CMOS PLA is realized by
- a. pseudo nmos NOR gate
 - b. CMOS NOR gate
 - c. pseudo nmos NAND gate
 - d. CMOS NAND gate
63. The mapping of irregular combinational logic functions into regular structures is provided by the
- a. FPGA
 - b. CPCD
 - c. standard cells
 - d. PLA
64. The general arrangement of PLA is
- a. AND/OR structure
 - b. OR/AND structure
 - c. NAND/NOR structure

d. EX-OR/OR structure

65. V XP X Z PLA represents as

a. V-no.of input variables

P-no.of output functions

Z-no.of gates

b. V-no.of gates

P-no.of OR gates

Z- no.of AND gates

c. V-no.of input variables

P-no.of product terms

Z-no.of output functions

d. V-no.of gates

P-no.of AND gates

Z-no.of output functions

66. To realize any finite state machine requirements, the PLA along with

a. NOR gate is used

b. feed back links is used

c. NAND gate is used

d. NOT gate is used

67. To reduce the PLA dimensions, the simplification must be done on a

a. individual output basis

b. multi-output basis

c. individual product term

d. individual input basis

68. The regularity of the PLA sturcture shows that both the AND and OR planes are constructed from

a. different standard cells

b. standard cells are not used

c. same standard cells

d. feed back control links

69. The behavior AND/OR structure of a system may be capured in

a. hardware description language

b. software language

c. tabulation method

d. state design model

70. VHDL differs from other software languages by including

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- a. behaviour of system
- b. compilers, debuggers and simulators
- c. syntax
- d. machine understanding language

71. The advantage of fuse-based FPGAs compared to other FPGAs is

- a. allows large number of interconnections
- b. complex fabrication process
- c. larger in size
- d. modified without changing hardware

72. Where the design is of moderate complexity and time to silicon is of paramount importance then the probably suitable approach is

- a. FPGA
- b. PLA
- c. standard cell
- d. PAL

73. A single time programmable FPGA is the type of

- a. fuse-based FPGA
- b. SRAM-FPGA
- c. EPROM-FPGA
- d. Flash based FPGA

74. The SRAM-FPGA's consists of a large array of programmable logic cells known as

- a. Erasable programmable logic devices-EPLD
- b. configurable logic blocks-CLB
- c. micro cells
- d. AND/OR array

75. The fabrication process of EPROM-FPGA is

- a. easy and high integration density
- b. easy and low integration density
- c. complex and high integration density
- d. complex and low integration density

76. The following is a chip whose final logic structure is directly configured by the end user

- a. gate array design
- b. field programmable logic
- c. standard cell design

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d. full custom design

77. FPGA can be programmed as per the

- a. positive logic**
- b. negative logic**
- c. users logic**
- d. fixed logic**

78. The logic cells in FPGA contains

- a. only combinational circuits**
- b. only sequential circuits**
- c. both combinational & sequential circuits**
- d. only Flip-Flop circuits**

79. The individual cells of FPGA are interconnected by

- a. AND gates and switches**
- b. matrix of wires and programmable switches**
- c. OR gates and non programmable switches**
- d. AND & OR gates**

80. The programming in fuse-based FPGAS is done by

- a. configurable logic blocks**
- b. memory cell**
- c. multiplexer**
- d. closing antifuse switches**

81. A slow rate control is used in the I/O block of CPLD because of

- a. matching with other parts**
- b. suppressing the occurrence of the noise**
- c. grounding the I/O pin**
- d. global tree state control**

82. Which part of the CPLD is programmed to pass the latched or unlatched, true or complement output to the external output

- a. AND gates of array**
- b. OR gates of array**
- c. I/O cell**
- d. standard cell**

83. A slow rate control in the I/O block of CPLD is used to make the rising and falling of the output pulse

- a. zero**
- b. one**

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c. faster

d. slow

84. A macro cell in CPLD is composed of

a. J-K flip-Flop

b. R-S Flip-Flop

c. T-Flip-Flop

d. D-Flip-Flop

85. CPLD devices are used for design modification because these are

a. reprogrammable

b. non programmable

c. always a fixed program

d. design modifications are not possible

86. CPLD is a device of numerous integrated SPLDs and interconnections between them is

a. non programmable

b. programmable

c. used single SPLD

d. permanent connections are used

87. To compose a circuit in case of CPLD, it has wiring among

a. the pins

b. the logic

c. connection on printed board

d. the function

88. CPLD is possible to rewrite it many times because

a. it records the contents of the circuit to the flash memory

b. a standard cell is used

c. it is a plastic loaded chip

d. it is AND/OR array

89. The CPLD can be rewritable in about

a. < 10 times

b. < 100 times

c. < 1000 times

d. > 1000 times

90. During programming of CPLD, the I/O pin is at the state of

a. logic 0

b. logic 1

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c. high impedance

d. open

91. The function block of CPLD consists of

a. AND array, OR array and macro cell

b. OR array, product term allocator and macrocell

c. AND array, product term allocator and marcocell

d. AND array, product term and OR array

92. In the standard cell, all the cells should have

a. identical heights and widths

b. identical heights and the widths of the cells may vary

c. identical widths and the variable heights

d. variable heights and widths

93. Cells in different rows of standard cells can be connected by using

a. internal wires

b. feed through cells

c. intra wires

d. route around a complete row

94. When a design is implemented in the standard cell design style

a. only signal routing has to be done

b. replacement of library cells

c. change of the design fucntion

d. change of placement of blocks

95. Standard cell designs are less area efficient than a full custom design due to

a. feed through cells

b. multiple cell rows

c. fixed size of the cells

d. lower clock rates

96. Where the design is of a reduced cost and include size memories the preferable approach is

a. FPGA

b. gate array logic

c. standard cell

d. full custom

97. Logic gates are placed in rows of standard cells of

a. equal height

b. equal width

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c. variable height

d. constant width

98. Logic gate are placed in rows of standard cells are interconnected using

a. internal wires

b. intra wire

c. routing channel

d. switch box

99. Semicustom design using standard cells enable the designes to use

a. a functional modules (available in library)

b. a layout automatically generated

c. an interconnections between cells

d. only basic logic functions

100. In the standard cell design methodology

a. each transistor is manually designed

b. predefined logic and function blocks are available

c. final logic structure is directly configured

d. an array of unconnected logic gates

101. Standard cell designs are operate at

a. higher clock rates and less area efficient

b. lower clock rates and less area efficient

c. lower clock rates and high area efficient

d. higher clock rates and high area efficient

102. PAL16R8, here R denotes the

a. number of inputs

b. number of outputs

c. active high

d. presence of flip-flop

103. PAL10L8, here L denotes the

a. active high

b. active low

c. number of inputs

d. number of outputs

104. If one function depend on other functions in PAL then

a. OR gate is used

b. feed back is used

c. ex-OR gate is used

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d. realization is not possible

105. One approach that is becoming more popular and feasible is to model chips as collections of

a. standard cells

b. no.of gates

c. reprogrammable gate arrays

d. semicustom design sub systems

106. Programmable array logic provide a convinient way of realizing

a. combinational networks only

b. sequential networks only

c. both combinational and sequential network

d. not used for realization

107. Programmable array logic is made up of

a. programmable AND and OR array

b. programmable AND and fixed OR array

c. Fixed AND and programmable OR array

d. Fixed AND and OR array

108. The number of product terms in PAL depends on

a. number of AND gates

b. number of OR gates

c. number of addition of both AND and OR gate

d. independent of number of gates

109. To realise the sequential networks in PAL, the type of flip-flop used is

a. D flip-flop

b. T flip-flop

c. J-K flip-flop

d. R-S flip-flop

110. The combination PAL devices with active-low outputs mean

a. AND-OR logic

b. AND-NOR logic

c. AND-NAND logic

d. NAND-OR logic

111. In order to realize a Boolean function with a combinational PAL device, the function must be expressed in

a. POS form

b. SOP form

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c. Standard form

d. complex form

112. When the PAL sequential device has a tristate buffer at the output stage then the type of circuit implemented is

a. sequential circuit

b. product terms

c. pos form

d. combinational circuit

113. An interface description of design entity in VHDL must define the

a. logical interface to the outside world

b. internal operations

c. organization of hardware

d. logical definition

114. The following is the Design flow through typical CMOS VLSI tools

a. Shown in figure (a)

Figure(a)

b. Shown in figure (a)

Figure(a)

c. Shown in figure (a)

Figure(a)

d. Shown in figure (a)

Figure(a)

115. VHDL was developed for the VHSIC components to

a. design and interchange format

b. simulation and fault analysis only

c. design description and simulation

d. certification and architectural evaluation

116. The primary abstraction in VHDL is called

a. interface description

b. body description

c. structural description

d. design entity

117. Each port declaration of design entity in VHDL includes a

a. hardware description

b. port name, associated mode and type

c. internal operations

d. logical functions

118. The component declarations in VHDL include an interface description for each of the

- a. signals**
- b. input port**
- c. output/port**
- d. logic gates**

119. VHDL provides high-level definition and simulation of

- a. simple digital systems**
- b. complex digital systems**
- c. standall cell design systems**
- d. analog systems**

120. The design is commenced with a

- a. RTL description**
- b. behavioral description**
- c. logic description**
- d. functional description**

121. Generally logic optimization systems divide the problem into

- a. technology dependent phase and technology mapping phase**
- b. technology independent phase and technology mapping phase**
- c. combinational circuits and sequential circuits**
- d. registers and logic gates**

122. Logic optimization is used to improve the logic to meet

- a. logic constraints**
- b. timing or area constraints**
- c. power constraints**
- d. parasitic constraints**

123. In the case of state-machines RTL compilers need to provide for

- a. automatic state assignment and minimization**
- b. trigger the registers on the rising edge of clock**
- c. set of logic gates**
- d. set of registers**

124. Logic optimization scheme converts the logic into a

- a. two level PLA POS form**
- b. standard form**
- c. two level PLA SOP form**

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d. combinational and Register circuits

125. Logic synthesis systems are very useful for

a. transforming between technologies

b. very good silicon implementation

c. to create control logic

d. to create micro code

126. Behavioral synthesis is

a. technology dependent and specify the implementation

b. technology independent and specify the implementation

c. technology independent and without specify the implementation

d. technology dependent and without specify the implementation

127. Which of the following synthesis converts RTL description to a set of registers and combinational logic

a. behavioral synthesis

b. RTL synthesis

c. logic level synthesis

d. layout synthesis

128. RTL description are captured using

a. hardware description language (HDL)

b. software description language

c. cathedral series

d. micro controllers

129. The wait statement of VHDL indicates the presence of

a. counters

b. logic gate

c. multiplexer

d. clocked register

130. The case operator of VHDL indicates the

a. counters

b. logic gate

c. multiplexer

d. clocked register

131. The delay of the gate in logic level simulators can be calculated as
the intrinsic gate delay (no load)

actual load in some units

the delay per load in some units

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a.

b. +

c. x +

d. + x

132. Standard cell and memory are simulated at the level of

a. both at logic level

b. both at functional level

c. logic level and functional level

d. functional & logic level

133. RTL simulations may be done with the actual clock timing by estimating the

a. layout loading capacitance

b. required speed of design

c. size of transistor

d. power dissipation in the circuit

134. The execution time of timing simulator compared to circuit simulators is

a. more

b. less

c. equal

d. not comparable

135. The layout is a faithful reproduction of the structure of the RTL description means

a. all the components are placed correctly

b. all signals are routed correctly

c. functionality is correct

d. system performs as required

136. Simulator of software tools is used to

a. compile the program

b. synthesize the given circuit

c. predict and verify the performance

d. transfer structural description to physical form

137. The most detailed and accurate simulation technique is

a. gate level

b. timing

c. logic level

d. circuit-level

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138. Circuit level simulators are characterized by

- a. high accuracy and long simulation time
- b. less accuracy and long simulation time
- c. high accuracy and short simulation time
- d. less accuracy and short simulation time

139. Circuit level & timing simulations evaluated on a timing sub step basis, where as logic-level simulation is

- a. applied voltage basis
- b. applied current basis
- c. event driven basis
- d. logic - level basis

140. Switch level simulators merge logic simulators techniques with some circuit simulation techniques by modeling transistors as

- a. gates
- b. open circuits
- c. short circuits
- d. switches

141. Switch - level simulators are combination of

- a. circuit level and timing simulators
- b. Circuit level and logic level simulators
- c. logic level & timing simulators
- d. gate and logic level simulators

142. YACR2 router is used to route the

- a. switch box
- b. maze
- c. rectangular channel
- d. global routing

143. The min-cut algorithm minimizes the area by

- a. splitting the conceptual layout until the leaf cells are reached
- b. minimize the SOP form of given function
- c. minimize the POS form of given function
- d. uses standard cells and proper floor planning

144. Maze routers can route any configuration but have comparatively

- a. short running time
- b. small area
- c. long running time

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d. large area

145. Interactive graphic editors are used to capture the

a. RTL circuit

b. behaviour of system

c. layout

d. structure of system

146. In layout synthesis generally two phases are required they are

a. designing and minimizing

b. placement and routing

c. optimization of logic and functioning

d. testing and verification

147. The traditional method of capturing a digital system design is

a. schematic editor

b. flow table

c. ASIC design

d. compiler

148. Many design systems allow diagrams because these are

a. more easy

b. quickly understood

c. small in size

d. small area

149. Many design systems generally use HDL because of

a. easy

b. quickly understood

c. small in size

d. easily modified

150. Schematic editors in digital design systems provide a

a. means to draw and connect components

b. compilation of code

c. simulation of system

d. synthesis of system

151. A layout editor might interface to a design rule checking program to allow interactive checking of

a. layout minimization

b. DRC errors

c. design errors

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d. possibility of transistor sizing

152. Floor plan editors provide graphical feed back about

a. size and placement of modules

b. internal layout details

c. connectivity of components

d. input / output port details

153. Pearl program analyzer is used to calculate

a. node voltages

b. loop currents

c. DRC errors

d. delays in circuit operation

154. The timing analyzer does not recognize some paths for some reasons

these paths are called

a. critical paths

b. crossed paths

c. sneak paths

d. long paths

155. Simulations with delays are used to check the

a. timing problems

b. DRC errors

c. functionality

d. speed of system

156. Pearl program analyzer is used to calculate

a. node voltages

b. loop currents

c. DRC errors

d. delays in circuit operation

157. Network isomorphism is used to prove that a layout is equivalent to

a. a network extracted from a schematic

b. optimum layout

c. optimized placement and routing

d. fabrication mask

158. Electron Beam exposure system is used to

a. create a data used for mask making

b. make a layout from net list

c. check the design rules

d. verify the timing analysis

159. A timing analyzer implemented at the transistor level can provide a designer

a. rapid global functional simulation

b. rapid feed back about critical paths

c. detailed module verification

d. details of DRC errors

160. Network isomorphism is used to prove that

a. two network are equivalent and therefore should function equivalently

b. the critical path in the system is the longest path

c. the layout satisfies the design rules

d. the design is optimum

161. The process of comparing two network is commonly called (indicate incorrect answer)

a. Layout versus schematic

b. network analysis

c. network isomorphism

d. netlist comparison

162. A design-rule-checker is used to

a. find DRC errors

b. conforms the layout to the geometric design rules

c. verify the functionality of the geometric design rules

d. verify the functionality of the design

163. The last step in the design process is

a. layout extraction

b. back annotation

c. pattern generation

d. design -rule verification

164. For MOS circuits the dominant faults are due to

a. short circuits in diffusion layers

b. open circuits in diffusion layer

c. short circuits in interconnections

d. open circuits in interconnections

165. Very effective aid to testing and testability of a design is

a. a reset facility

b. facility to probe the circuit nodes

c. provide circuit modification

d. sealed in over glass

166. Correct operation of a design must not be dependent on

a. Rise times or fall times

b. short circuits in diffusion layer

c. Layout

d. short and open circuits in metal layer

167. Generally functional tests are impractical due to

a. fast simulation times and short verification sequences

b. fast simulation times and long verification sequences

c. slow simulation times and very long verification sequences

d. slow simulation times and short verification sequences

168. During testing of VLSI system (Indicate the false statement)

a. The chip is sealed by an overglass layer

b. circuits nodes cannot be probed for monitoring

c. circuits can be modified

d. circuits cannot be modified

169. Generally the amount of chip area dedicated for testability is

a.

b.

c.

d.

170. The advantage of a reset facility in the design is

a. testing always from fixed position

b. testing proceed from known enditions

c. testing proceed from unknown conditions

d. It is not related to testing

171. A 20 bit counter is split into four five bit section, them the required steps for testing are

a.

b. four sets of 2^5

c. five sets of 2^4

d. five sets of 2^5

172. Manufacturing tests are used to verify that

a. function of a chip as a whole

b. every gate operates as expected

c. function in the field

d. the clock response of the chip

173. VHDL, verilog hardware description languages are used for testing of

a. manufacturing tests

b. functionality test

c. Design testing

d. chip testing

174. Functionality tests seek to verify the

a. function of a chip as a whole

b. every gate operates as expected

c. function in the field

d. the clock response of the chip

175. Adhoc testability means

a. testability arrangements configured with the architecture changes

b. testability with structure changes

c. testability arrangements configured without changing the architecture

d. testability without structure changes

176. A measure of goodness of a test program is

a. the amount of fault coverage

b. time

c. cost

d. degree of performance

177. At the prototype state it is possible to provide special test points by

a. providing extra pads for probing

b. It is not possible to test

c. modifying the circuit

d. link connections

178. A finite state machine with 'n' possible inputs to the combinational logic and 'm' memory elements then the required test vectors are

a. $m + n$

b. 2^m

c. 2^n

d.

179. Generally the system is partitioned for testing because

a. reducing the chip area

b. reducing the no. of pads

c. reducing the number of test vectors

d. reduce the required power

180. The two key concepts underlying all considerations for testability are

a. set and reset

b. controllability and observability

c. initial and final conditions

d. pads and links

181. Controllability in testing means

a. being able to set known internal states

b. being able to generate all states

c. being able to generate all combinations of circuit states

d. read out the result of the state changes

182. Being able to generate all states to fully exercise all combinations of circuit states is called

a. controllability

b. observability

c. combinational testability

d. reset facility

183. Being able to read out the result of the state changes as they occur is called

a. controllability

b. reset facility

c. combinational testability

d. observability

184. The faults occur due to thin-oxide shorts or metal-to-metal shorts are called

a. stuck-at-zero faults

b. short-circuit faults

c. open-circuit faults

d. bridge faults

185. Random logic is probably best tested via

a. self testing

b. full serial scan or parallel scan

c. boundary scan

d. LFSR method

186. Self-test circuitry approach is based on

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- a. linear feed back shift registers only
 - b. linear feed back shift registers, exclusive-OR and clock system or gate
 - c. clock system only
 - d. enclusive OR gates only
187. The combination of LSSD scan path and linear feed back shift register is called
- a. self test circuitry
 - b. signature analysis technique
 - c. structured testbility
 - d. built-in logic block observation
188. In the following which one is corrcet with respect to BILBO testing for control inputs $C_0=1$, $C_1=1$
- a. linear shift mode
 - b. signature analysis mode
 - c. data latch
 - d. reset mode
189. The control inputs in BILBO testing the coresponding mode is
- a. linear shift mode
 - b. signature analysis mode
 - c. datalatch
 - d. reset mode
190. In the BILBO arrangements, when $C_0=0$, $C_1=1$ then the corresponding mode is
- a. linear shift mode
 - b. signature analysis mode
 - c. data latch
 - d. reset mode
191. The following the mode when $C_0=1$, and $C_1=0$ in the BILBO arrangement
- a. linear shift mode
 - b. signature analysis mode
 - c. data latch
 - d. reset mode
192. On chip testing is obtained by using
- a. self - test circuitry
 - b. adhoc testability
 - c. structured testability

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d. LSSD approach

193. Signature analysis techniques are

- a. on chip testing**
- b. structured testing**
- c. LSSD testing**
- d. adhoc testability**

194. The manufacturing cost is low by detecting the malfunctioning of chip at a level of

- a. wafer level**
- b. packaged-chip**
- c. system level**
- d. field**

195. The tests that are usually carried after chip is manufactured are called

- a. functionality test**
- b. design verification**
- c. manufacturing test**
- d. technology test**

196. Generally memories are tested by

- a. self-test**
- b. full serial scan**
- c. parallel scan**
- d. LFSR method**

197. In order to reconfigure flip - flops appropriately, it is necessary to be able to include a double throw switch in the

- a. simple scan path**
- b. address path**
- c. control singnal path**
- d. data path**

198. The test access port or TAP controller in a boundry - scan system level testing is a

- a. 16 - state FSM**
- b. 8 - state register**
- c. 8 - state interface pins**
- d. 16 - state NAND gates**

199. The following path is used to reduce testing time in the LSSD

- a. simple scan path**

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b. parallel path

c. single path

d. complex path

200. The test access port or TAP controller in a boundary - scan system - level testing has connections of

a. one single bit

b. one multiple bits www.studentmoments.com

c. four or five single bit

d. one or two multiple bits

201. The insuction register (IR) in boundry-scan system level testing has to be at least

a. one bit long

b. two bit long www.studentmoments.com

c. there bit long

d. four bit long

202. Subsystems can be checked out individually by providing the appropriate

a. additional inlet/outlet pads

b. additional circuit nodes

c. additional links

d. It is not possible to check

203. The essence of the LSSD approach is to design all circuitry in a

a. transistor to transistor

b. transistor to register

c. register to register

d. register to transistor

204. In the structured testing technique, LSSD means

a. level scan sensistive default www.studentmoments.com

b. level simple scan design

c. level scan simple default

d. level sensitive scan design

205. In the LSSD approach the resisters behaves like a

a. shift register in operation mode and latch in testmode

b. shift register in test mode and latch in operation mode

c. shift registers in both test and operation mode

d. latch in both test and operation mode

206. The IEEE 1149 boundary scan is used for

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- a. chip level testing
- b. design test
- c. system level testing
- d. circuit level testing

207. To increase the immunity to open - circuit faults usually involve incorporating

- a. misaligned
- b. connection redundancy
- c. nature of defects
- d. frequency of defects

208. To find the bridging faults, the following popular testing method is used

- a. scan testing
- b. I L A
- c. I D D Q
- d. self testing

209. The layout is tested by using

- a. Design rule checker www.studentmoments.com
- b. simulator
- c. PROBE
- d. BILBO

210. The layout modifications improves the performance

- a. typically 10 % - 20 %
- b. greatethan 50 %
- c. typically 100 %
- d. typically 30 % to 50 %

211. NET is used to

- a. verify its compliance with the design rules
- b. extract the circuit from the mask layout
- c. test for the number of contacts
- d. simulate the leaf cell

212. PROBE is used to

- a. verify the design rules
- b. extract the circuit from the mask layout
- c. layout testing
- d. simulate the cell

213. To reduce parasitics, the changes are made in

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- a. circuit
- b. transistor size
- c. layout
- d. logic

214. The steady state response to any allowed input state change is independent of the circuit and wire delays within the system then this logic system is called

- a. level-sensitive
- b. finite state machine
- c. stable - state
- d. combinational logic circuit

215. Long counters are tested by

- a. scan - based approaches
- b. self test
- c. built - in testing
- d. ad-hoc testing

216. The following type of a fault should not disturb the functionality of the circuit

- a. Delay fault
- b. bridge fault
- c. open circuit
- d. stuck at faults

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